## REMARKS

This paper is submitted in reply to the Office Action dated October 6, 2006, within the three-month period for response (as January 6, 2006 is a Saturday). Reconsideration and allowance of all pending claims are respectfully requested.

In the subject Office Action, claims 7-9, 12-14 and 30-31 were rejected under 35 U.S.C. § 101. Additionally, claims 1, 3,4, 10-11, 1-7, 19 and 24-31 were rejected under 35 U.S.C. § 102(b) as being anticipated by Enhanced Simulated Annealing for Automatic Reconfiguration of Multiprocessors in Space by James R. Slagle et al., ACM 1989 (hereinafter "Path"), and claims 2, 5-6, 18 and 20-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Path in view of U.S. Patent No. 6,971,092 to Chillimibi (hereinafter "Cache").

Applicant respectfully traverses the Examiner's rejections to the extent that they are maintained. Applicant has amended claims 17, 20-27 and 29-31, and Applicant submits that no new matter is being added by the above amendments, as the amendments are fully supported in the specification, drawings and claims as originally filed.

As an initial matter, the Examiner will note that claims 17, 20-27 and 29 have been amended for clarification purposes, and specifically to distinguish between "first" and "second" program code, in a similar manner to claim 30 as filed. Applicant notes that these amendments do not affect the scope of these claims in any appreciable manner.

Now turning to the subject Office Action, and initially to the §101 rejection of claims 30 and 31 as being directed to non-statutory subject matter, the Examiner will note that Applicant has amended claim 30 to recite a "physical computer readable medium," and amended claim 30 to clarify that the physical computer readable medium is a "recordable" medium. Applicant is under the impression that this language complies with the Office's current interpretation of §101, and accordingly, withdrawal of the §101 rejection of claims 30-31 is respectfully requested.

With regard to the §101 rejection of claims 7-9 and 12-14 as lacking patentable utility, Applicant first traverses this rejection on the basis that it is improper as a matter of law to reject a dependent claim under 35 U.S.C. §101 when the underlying independent claim is considered to be statutory. Since a dependent claim necessarily incorporates all

of the limitations of its parent, independent claim, the subject matter in an independent claim that renders that claim statutory is also necessarily present in the dependent claim. Put another way, it is impossible for the additional language recited in a dependent claim to "undo" the statutory nature of the claim as a whole, given that claim includes inherited language from a parent claim that has otherwise been found to be statutory.

In addition, specifically with regard to the rejected claims, the Examiner apparently considers these claims to lack utility because they call out randomization, which, in the Examiner's opinion, produces non-deterministic results. The fact that randomization is used in a claimed method, however, does not render the results of that method indeterminate as a whole. As an example, one type of optimization algorithm that relies on random selection, and which is described in the application and recited in claim 3, is a "simulated annealing" algorithm. The Examiner's attention is respectfully directed to the definition of "simulated annealing" on the National Institute of Standards and Technology site (http://www.nist.gov/dads/HTML/simulatedAnnealing.html), which defines simulated annealing as "[a] technique to find a good solution to an optimization problem by trying random variations of the current solution." (*emphasis added*). Indeed, the fact that claim 3 (which calls out simulated annealing, an algorithm that relies in part on randomness) is not rejected under §101 is inconsistent with the Examiner's position.

Furthermore, an algorithm that relies on simulated annealing or randomness is neither indeterminate nor is it of unknown utility, because the algorithm as a whole still produces a concrete result. In fact, as discussed at page 7 of the application, an advantage of simulated annealing and other algorithms incorporating randomness is the fact that the algorithm is often better able to converge on a global optimal result, rather than converging on a local solution that may not be optimal from a global standpoint. Applicant also submits that given the wide variety of algorithms in existence that rely in part on randomness (including, in addition to simulated annealing, genetic programming algorithms, neural networks, fuzzy logic, etc.), it is well established that useful, concrete, and deterministic results can be obtained using an algorithm that relies in part on randomness. Indeed, even the first page of the Path reference, which is used to reject the claims under §§102 and 103, touts the utility of simulated annealing and similar

randomness-based algorithms. Accordingly, reconsideration and withdrawal of the §101 rejection of claims 7-9 and 12-14 is respectfully requested.

Next turning to the art-based rejections, and specifically to the rejection of claim 1, this claim generally recites a method of ordering program code in a computer memory. The method includes selecting an ordering from among a plurality of orderings for a plurality of program code segments using a heuristic algorithm, and ordering the plurality of program code segments in a memory of a computer using the selected ordering.

Path, in contrast, discloses the use of simulated annealing to map logical processors to physical processors in a multiprocessor system, in particular, a space borne processor array (SPA) (page 401). Path, however, is completely silent with respect to the use of a simulated annealing algorithm, or any other type of algorithm, to order program code in a computer memory, as is recited in claim 1. The claim also recites "selecting an ordering . . . for a plurality of program code segments" and "ordering the plurality of program code segments in a memory of a computer," neither of which is disclosed by Path. The assignment of logical processors to physical processors, as disclosed in Path, does not order program code segments in a computer memory. Applicant can find no disclosure in the description of the SPA hardware design (found in page 2 of Path) that is relevant to the concept of ordering program code segments within a computer memory.

In order to anticipate a claim, a reference must disclose each and every feature recited in the claim. Accordingly, Applicant submits that Path fails to anticipate claim 1, as the reference fails to disclose the concept of ordering program code segments in a computer memory, much less doing so based upon a heuristic algorithm. Withdrawal of the Examiner's rejection of claim 1 is therefore respectfully requested.

In addition, Applicant submits that claim 1 is non-obvious over Path and the other prior art of record, as there is no suggestion in the art to modify Path to use simulated annealing or another heuristic algorithm to order program code segments in a memory. As noted above, Path uses simulated annealing to assign logical processors to physical processors, and does not disclose ordering program code segments. Furthermore, to the extent that the assignment of a logical processor to a physical processor may have an impact on the location of program code running on the logical processor, it should be

noted that claim 1 recites selecting from different orderings of program code segments using a heuristic algorithm. Even if a different assignment of a logical processor to a physical processor were to incidentally impact the location of program code in a physical processor, the algorithm disclosed in Path does not ever select from among different orderings of program code segments using a heuristic algorithm.

The other art of record, such as the cited Cache reference, similarly provides no motivation to modify Path. Cache, which the Examiner relies upon for allegedly disclosing the optimization of the use of a cache, is directed to identifying hot data streams, i.e., frequent accesses to data. Col. 7, lines 5-17, for example, disclose identifying sequences of consecutive data references. It is important to note, however, that these hot data streams are not relevant to the ordering of program code segments in a memory. Hot data streams are detected based upon the location of data accesses by program code, however, there is no concern in the reference for the location of the program code that makes such data accesses. Put another way, Cache is concerned with the fetching of data requested by program code instructions, but not the fetching of the instructions themselves.

Furthermore, neither Path nor Cache even address the same problem as is addressed by the invention recited in claim 1. Path is concerned with minimizing communication path length in a physical processor array, and speaks nothing of attempting to improve memory access performance related to the execution of program code through the ordering of program code segments in a memory. Cache is directed to data access patterns, and does not address the ordering of program code in a memory. Applicant therefore submits that one of ordinary skill in the art would not be motivated to modify Path to improve the memory access performance of an executed program based upon the ordering of program code in a memory.

Applicant therefore respectfully submits that claim 1 is non-obvious over Path, Cache and the other prior art of record. Reconsideration and allowance of independent claim 1, and of claims 2-16 which depend therefrom, are therefore respectfully requested.

Next, turning to the rejections of independent claims 17 and 30, each of these claims recites in part first program code configured to optimize execution of second

program code in a computer of the type including a multi-level memory architecture by using a heuristic algorithm to select an ordering from among a plurality of orderings for a plurality of program code segments in the second program code. As discussed above in connection with claim 1, this combination of features is not disclosed or suggested by Path or the other prior art of record. Independent claims 17 and 30 are therefore novel and non-obvious for the same reasons as presented above for claim 1. Reconsideration and allowance of independent claims 17 and 30, and of claims 18-29 and 31 which depend therefrom, are therefore respectfully requested.

Finally, Applicant traverses the Examiner's rejections of the dependent claims based upon their dependency on the aforementioned independent claims. Nonetheless, Applicant does note that a number of these claims recite additional features that further distinguish these claims from the references cited by the Examiner. However, in the interest of prosecutorial economy, these claims will not be addressed separately herein.

In summary, Applicant respectfully submits that all pending claims are novel and non-obvious over the prior art of record. Reconsideration and allowance of all pending claims are therefore respectfully requested. If the Examiner has any questions regarding the foregoing, or which might otherwise further this case onto allowance, the Examiner may contact the undersigned at (513) 241-2324. Moreover, if any other charges or credits are necessary to complete this communication, please apply them to Deposit Account 23-3000.

Respectfully submitted,

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Date

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